What is claimed is:

Sub a4

1. A CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of rows and columns, and image sensor logic on said substrate, said logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor other than said rows individually,

said substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge,

said image sensor extending between said first edge, said second edge, and said third edge, with no circuitry being located between said image sensor and any of said first, second or third edges, such that a first area adjacent said first edge of the chip includes first pixels of the image sensor; a second area adjacent said second edge of the chip includes image sensors, and a third area adjacent said third edge of the chip includes image sensors,

said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor.

2. A circuit as in claim 1 wherein said row logic is formed in place of two columns of the array forming the active pixel sensor.

3. A circuit as in claim 1 wherein said image sensor extends within two pixel pitches of first, second, and third edges of the chip.

4. A circuit as in claim 3 wherein said first and second edges are perpendicular to said third and fourth edges.

5. A circuit as in claim 1 further comprising an interpolation element, operating to interpolate pixels which would have impinged on areas of said image sensor portion.

6. A circuit as in claim 1 wherein said row logic is in the center of the plurality of pixels forming the image sensor.

7. A circuit as in claim 1 wherein the ends of the image sensor includes a guard ring.

8. A method of operating a large format image sensor, comprising:

first obtaining an image sensor chip which has first and second edges where said image sensor comes within two pixel pitches of said first and second edges, and includes row selecting logic in place of a plurality of central pixels of the image sensor;

abutting said image sensor chip against a similar image sensor chip of corresponding construction; and

interpolating missing pixels caused by both said row select logic and by spaces between said image sensor chips.

ADD A5

ADD 31

ADD D1